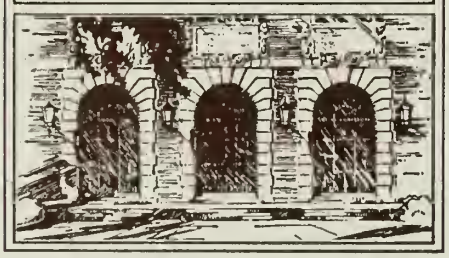

Report No. 188

HYBRID CIRCUITS FOR THE PARAMATRIX SYSTEM

by

Edward F. Prozeller

September 7, 1965

DEPARTMENT OF COMPUTER SCIENCE · UNIVERSITY OF ILLINOIS · URBANA, ILLINOIS

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1. INTRODUCTION

Currently under development in the Task 15 Group of the Digital Computer Laboratory is a pattern processing system called Paramatrix. The inputs to Paramatrix consist of line drawings which have been encoded into a discrete set of 32 d-c voltages lying in the interval +8 to -8 volts. The output of the system consists of the visual presentation of the input pattern, renormalized in position, size and azimuth. Hence, apart from input-output, the purpose of Paramatrix is to sequentially translate, rotate, and/or magnify a bounded set of analog voltages. The transformed analog data are then digitized in order that they can be used by a digital computer or, as in the present system, to drive a matrix of flipflop circuits for the purpose of visual display.

Obviously the above operations can be performed by a digital computer provided the input patterns have been digitized. Equally apparent however is the ease with which the above transformations can be achieved using high-speed analog techniques, namely, rotation from a sine-cosine potentiometer, magnification from an ultra-linear d-c amplifier and finally translation by means of d-c level shifting. In the Paramatrix system we have attempted to combine the advantages of both analog and digital techniques. The result is a special-purpose analog-digital computer in which the information signals are analog and the control signals are digital.

In order to realize the Paramatrix system it was necessary to design three types of circuitry. First the system required conventional digital circuits for timing and scanning. The second requirement was for for ultra-compensated analog circuits capable of handling the system information with great precision (negligible loss) and at a fast sampling rate (100 KC or better). Finally, the requirements called for rather elegant

analog-digital (hybrid) circuits in order to achieve digital-to-analog conversion and analog comparison.

The purpose of this thesis is to describe in detail the design of two hybrid circuits, namely, an analog gate and an analog comparator. In addition the design of a precision analog circuit, namely, a compensated emitter-follower, will also be discussed. Finally, a brief description will be given of the applications of these three circuits in a hybrid system like Paramatrix.

2. DIAMOND GATE

2.1 Circuit Requirements and Possible Solution

The first hybrid circuit required by the Paramatrix system was an analog gate. This is essentially a switch which is shorted when a digital signal is applied and open at all other times.

It was required that the switch be more ideal than the conventional transistor model since an absolute offset greater than 80 mv could not be tolerated. In addition it was necessary to gate voltages over the unusually wide range of -8 to +8 volts.

A circuit which is often used for voltage gating in analog computers is shown in Figure 1. In this circuit the bridge is biased on from t_0 to t_1 and if $v_s = 0$ and the diodes are matched, it is reasonable to assume

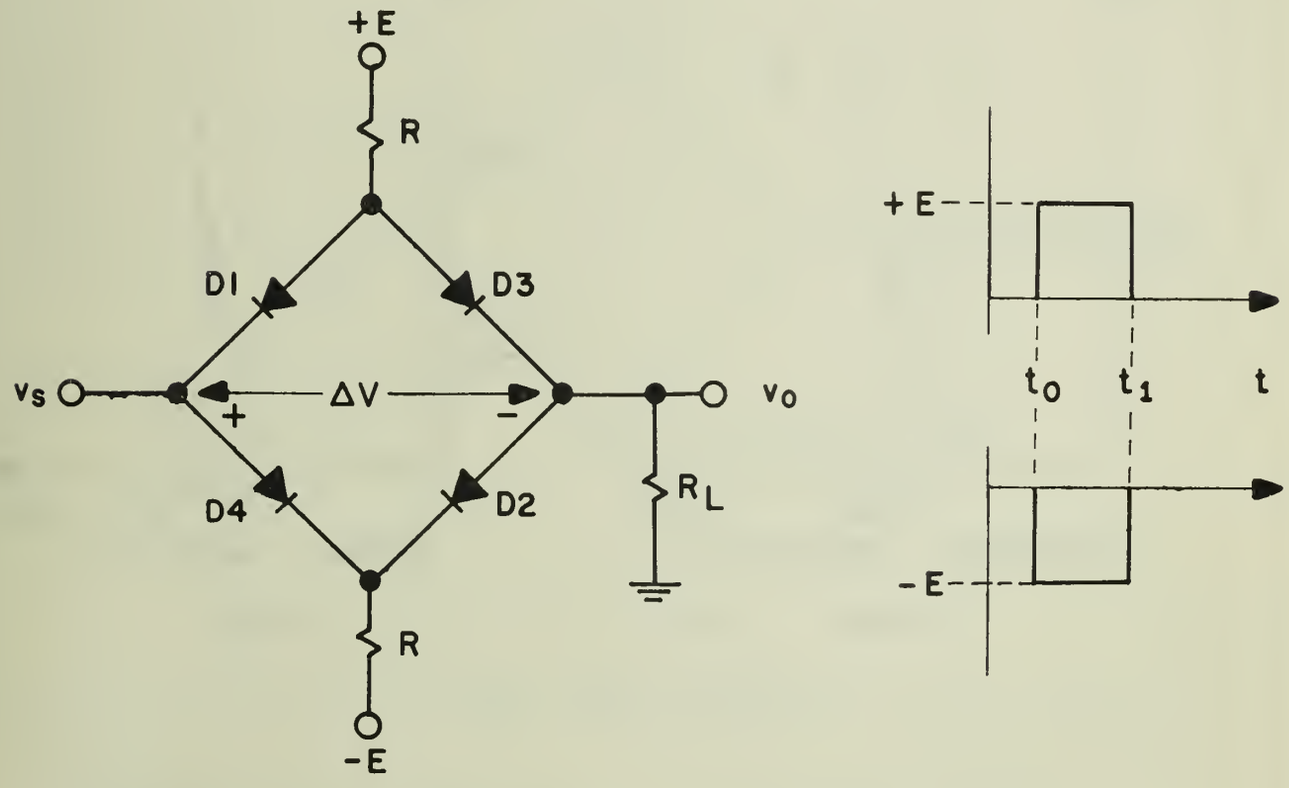

Figure 1. Conventional Analog Gate.

that the current through each diode is

$$I_{DQ} \simeq \frac{E}{2R} \tag{2.1}$$

If the usual diode curve of Figure 2(a) is assumed for each bridge diode and an offset $\Delta V = v_s - v_o$ is defined, then visibly $\Delta V = 0$ for the quiescent condition $v_s = 0$. Figure 2(b) shows the changes in the diode currents when a positive input signal is applied. In this case a voltage offset is encountered since D_1 now conducts less current and D_3 more. However, the offset is substantially less than the drop across a single diode because of the complimentary connection.

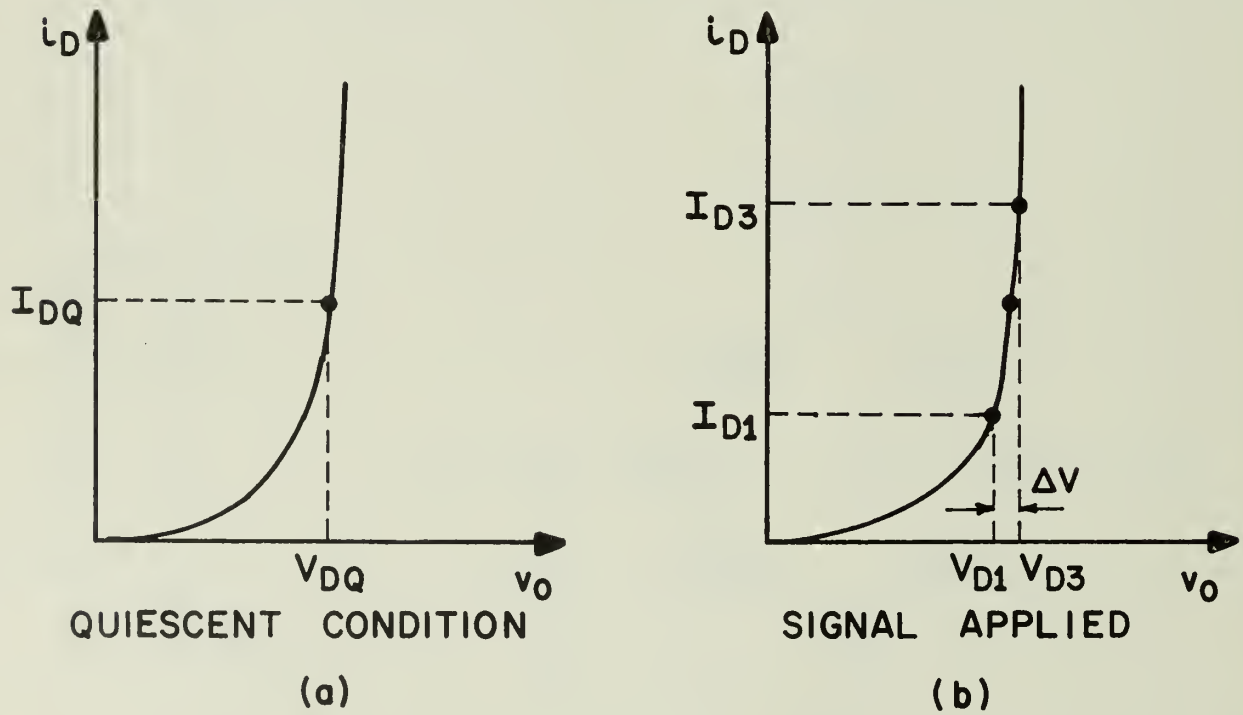

Figure 2. Diode Curves.

The main consideration in the design of a precision analog gate is to minimize the offset ΔV. In the diamond gate of Figure 1 minimum ΔV is achieved when I_{DQ} is maximum since in this case $\frac{dV}{dI}$ is minimum. To achieve a large I_{DQ} either E must be made large and/or R small.

2.2 Circuit Analysis

A simplified analysis can be made of the diamond circuit if it is assumed that all diodes conduct with negligible forward resistance and we neglect any source impedance. In this case the absolute maximum value of v_s as a function of E can be calculated such that all the bridge diodes conduct. As before, the quiescent diode current equals $\frac{E}{2R}$ and if all diodes are to conduct, the signal current i_s through the input diode D_1 (for positive input) must not exceed I_{DQ}. An a-c equivalent circuit for Figure 1 is given in Figure 3. From this model the signal current i_s is found to be

$$i_s = \frac{v_s(2R_L + R)}{2RR_L} \tag{2.2}$$

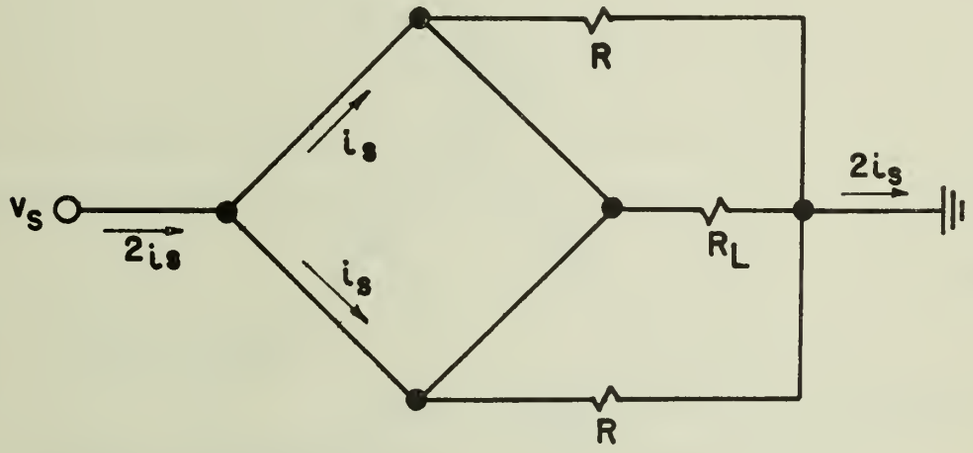

Figure 3. A-C Equivalent Circuit for Analog Gate.

The condition for the bridge to be biased on then becomes from Eq. (2.2) and $i_s < I_{DQ}$

$$\frac{v_s(2R_L + R)}{2RR_L} < \frac{E}{2R} \tag{2.3}$$

For a symmetrical signal swing about ground it is easy to see that condition (2.3) becomes

$$|v_s| < \frac{ER_L}{2R_L + R} \tag{2.4}$$

Equation (2.4) merely gives the condition that all diodes conduct; however, for low offset it is required that all diodes conduct well above the knee on the characteristic curve. It is reasonable therefore to state the condition for low offset as

$$|v_s| < \frac{1}{4} \left(\frac{ER_L}{2R_L + R}\right)$$

If in the above equation, $R_L \gg R$, then

$$|v_s| < \frac{1}{8} (E) \tag{2.5}$$

and if $|v_s| = 8$ v (as required), $E > 64$ v. Two bias supplies of this size is quite unreasonable, especially since, in order to switch the circuit, these biases must be switched.

2.3 The Method of Constant-Current Bias

Because of the unusually large signal swings required it became necessary to invent a more elegant method of biasing the diamond. It is logical that if a large quiescent current is maintained in the diodes independent of signal current then a constant-current bias will give a satisfactory solution.

Assuming a constant-current bias I_0 and an exponential v-i characteristic for the bridge diodes, it is possible to derive an equation for the bridge offset, ΔV, as a function of I_0 and i_s. Consider the circuit of Figure 4. Under the above assumption each of the diodes obey the equation

$$I_j = I_{sj} \left(e^{qV_j/KT} - 1\right) \qquad j = 1,2,3,4 \tag{2.6}$$

or

$$V_j = \frac{KT}{q} \ln \left(1 + \frac{I_j}{I_{sj}}\right) \tag{2.7}$$

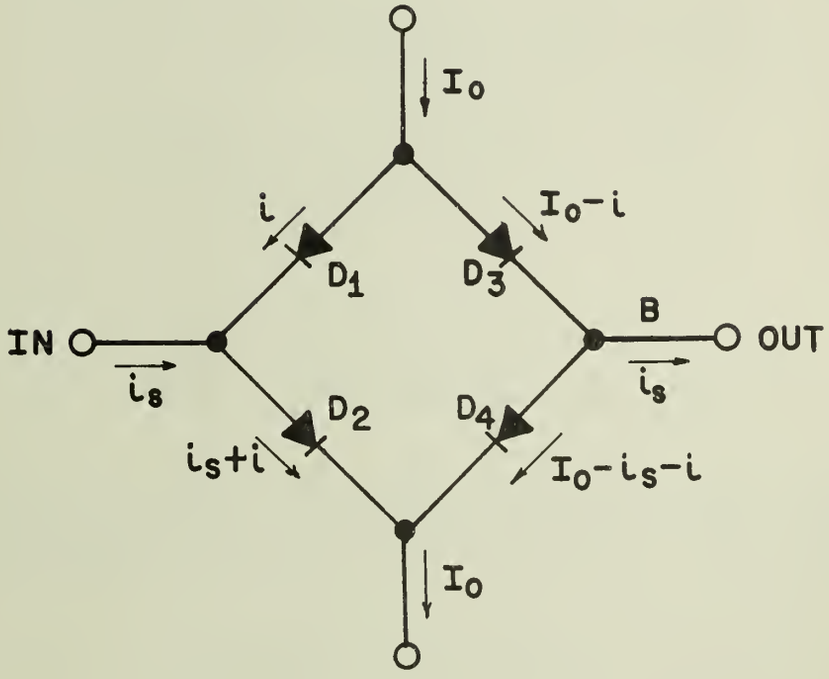

Figure 4. Analog Gate with Constant-Current Bias.

where in the above:

I_j = current through jth diode

V_j = voltage drop of jth diode

I_{sj} = saturation current for jth diode

K = Boltzman's constant

T = temperature (assume constant and equal for all diodes)

q = magnitude of electronic charge

Writing $I_1 = i$, it follows that $I_2 = i_s + i$, $I_3 = I_0 - i$ and $I_4 = I_0 - i_s - i$, as shown. The condition that $V_1 + V_2 = V_3 + V_4$ gives, from (2.7)

$$(1 + \frac{i}{I_{s1}})(1 + \frac{i_s + i}{I_{s2}}) = (1 + \frac{I_0 - i}{I_{s3}})(1 + \frac{I_0 - i_s - i}{I_{s4}}) \qquad (2.8)$$

It is most instructive to consider the solution of Eq. (2.8) when all diodes are identical, i.e., when $I_{s1} = I_{s2} = I_{s3} = I_{s4}$. The quadratic term in (2.8) then drops out and the unique solution is

$$i = \frac{1}{2}(I_0 - i_s) \qquad (2.9)$$

Thus

$$I_1 = I_4 = \frac{1}{2}(I_0 - i_s) \quad \text{and} \quad I_2 = I_3 = \frac{1}{2}(i_s + I_0) \qquad (2.10)$$

It is also interesting to note that if each diode is assumed to have a small series ohmic resistance r, Eq. (2.7) would be replaced by

$$V_j = \frac{KT}{q} \ln (1 + \frac{I_j}{I_{sj}}) + rI_j \qquad (2.11)$$

The solutions (2.10) still hold for identical diodes; however Eq. (2.11) is probably a more realistic equation for a real diode.

We are mainly interested in the voltage offset ΔV which becomes

$$\Delta V = V_3 - V_1 = V_4 - V_2 \tag{2.12}$$

It is convenient to make two approximations:

(a) that $I_0 - |i_s| \gg I_s$, which is almost certain to be true if all diodes are forward biased;

(b) that $i_s \ll I_0$, which may or may not be true.

Then from (2.11), (2.12) and (a)

$$\Delta V = \frac{KT}{q} \ln \frac{I_0 + i_s}{I_0 - i_s} + r\, i_s \tag{2.13}$$

If (b) is also true, (2.13) can be simplified still further since,

$$\ln \left(\frac{I_0 + i_s}{I_0 - i_s}\right) \simeq \ln \left(1 + \frac{2i_s}{I_0 - i_s}\right) \simeq \frac{2i_s}{I_0} \tag{2.14}$$

Thus Eq. (2.13) becomes

$$\Delta V \simeq \left(\frac{2KT}{qI_0} + r\right)\, i_s \tag{2.15}$$

It is useful to define a figure of merit for the circuit with constant-current bias, namely

$$R_\diamond \simeq \frac{\Delta V}{i_s} \simeq \frac{2KT}{qI_0} + r = \text{constant} \tag{2.16}$$

It will be noted that this figure of merit is in ohms and is equal to the magnitude of offset voltage divided by the load current (load current equals

signal current when constant-current bias is used). Obviously, the lower the figure of merit, the better the circuit.

The realization of a diamond gate with constant-current bias is actually quite straightforward. A realizable topology is shown in Figure 5.

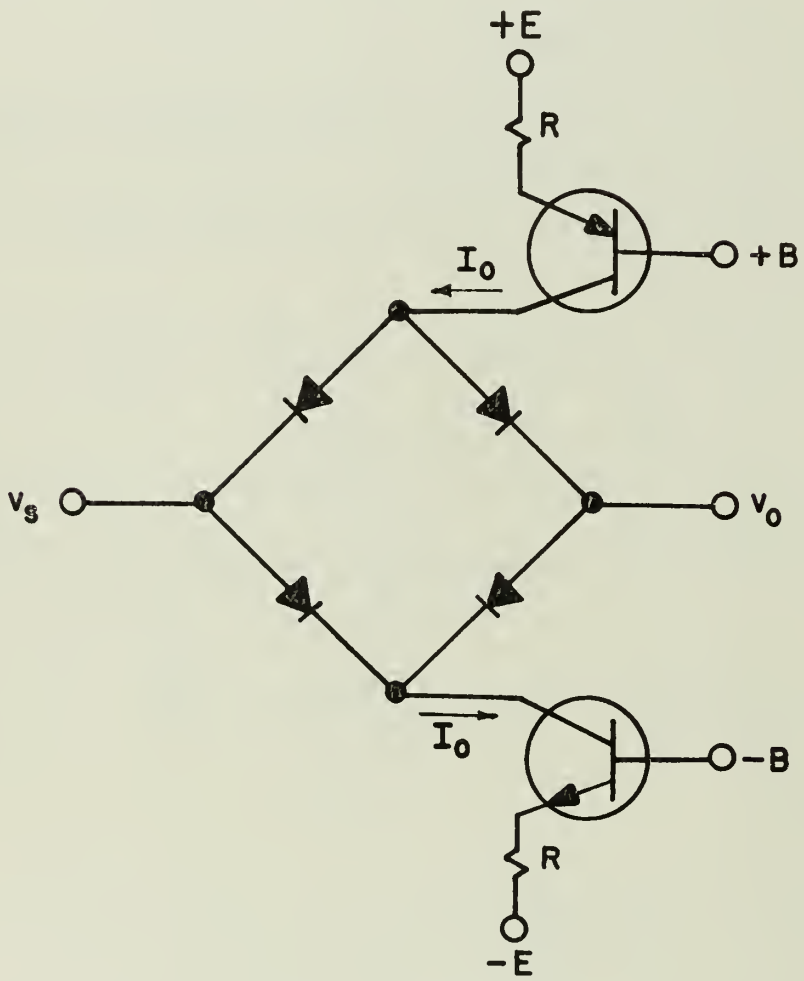

Figure 5. Diamond Gate with Current Generators.

In this circuit the bias current I_0 is approximately equal to $\frac{E-B}{R}$ and the collectors of the driver transistors can swing about $\pm$ B volts before an intolerable change occurs in I_0. Hence the requirement on v_s has now been reduced to $|v_s| < B$ which is easier to achieve than the conditions given by Eq. (2.5).

2.4 The Method of Bypass-Gating

In order to switch the circuit of Figure 5 most efficiently (i.e., no power is dissipated when the bridge is off) it is necessary to cut off the transistors by applying voltage pulses of magnitude +C and -C (where $|C| > E$) to the bases of T_1 and T_2 respectively. This is undesirable because it would require a power supply greater than E which is already large due to the offset requirements of the diamond.

An alternate method of switching the diamond, called Bypass-Gating, is shown in Figure 6. When transistor T_3 is on, T_1 and T_2 are held off and I_0 flows through T_3 instead of the bridge and the output v_0 essentially floats. When T_3 is off the bridge is biased and

$$v_0 = v_s + \Delta V \ .$$

The resistors R_1, R_2 serve to bias the zener which shifts the gate voltage to a level sufficient to control transistor T_3.

2.5 Diamond Gate for Paramatrix

The final diamond gate designed for the Paramatrix system is of the above type and is shown in Figure 7. The quiescent bridge current, I_0, is 15 ma and the results of a static test of this circuit are given in Table 1 and plotted in Figure 8.* The figure of merit, $R_\Diamond$, for this design

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* A quiescent offset ΔV_0 exists because the bridge diodes are not perfectly matched.

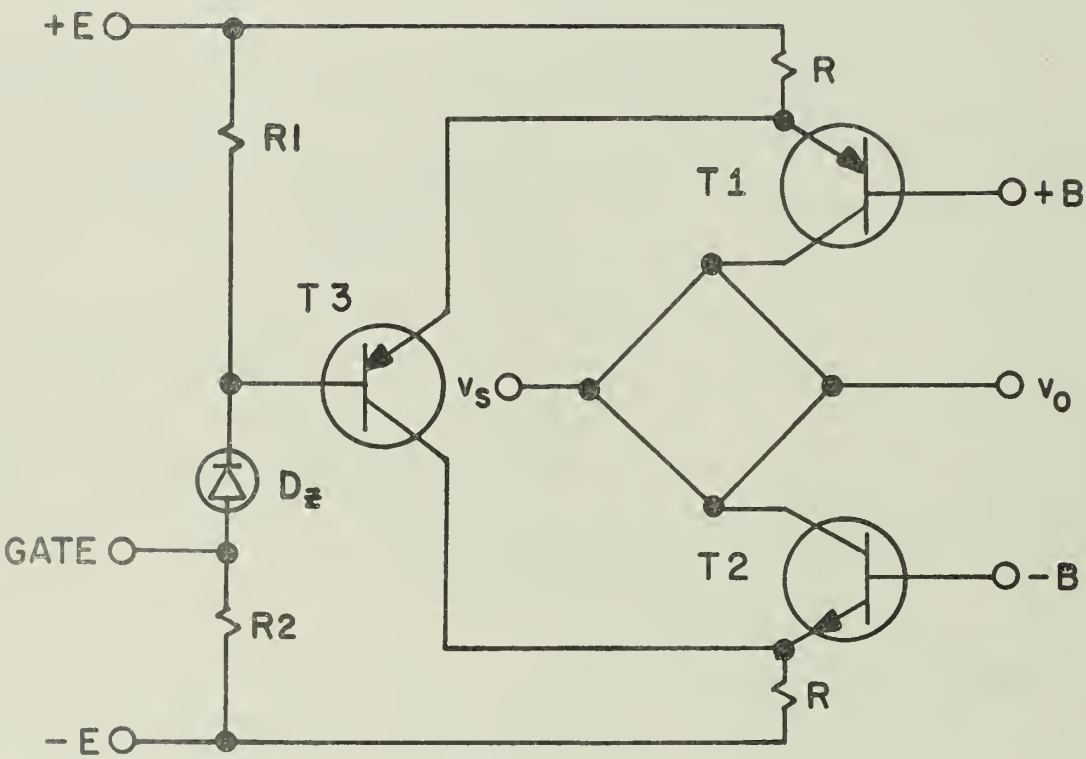


Figure 6. Bypass-Gating of Current-Driven Diamond.

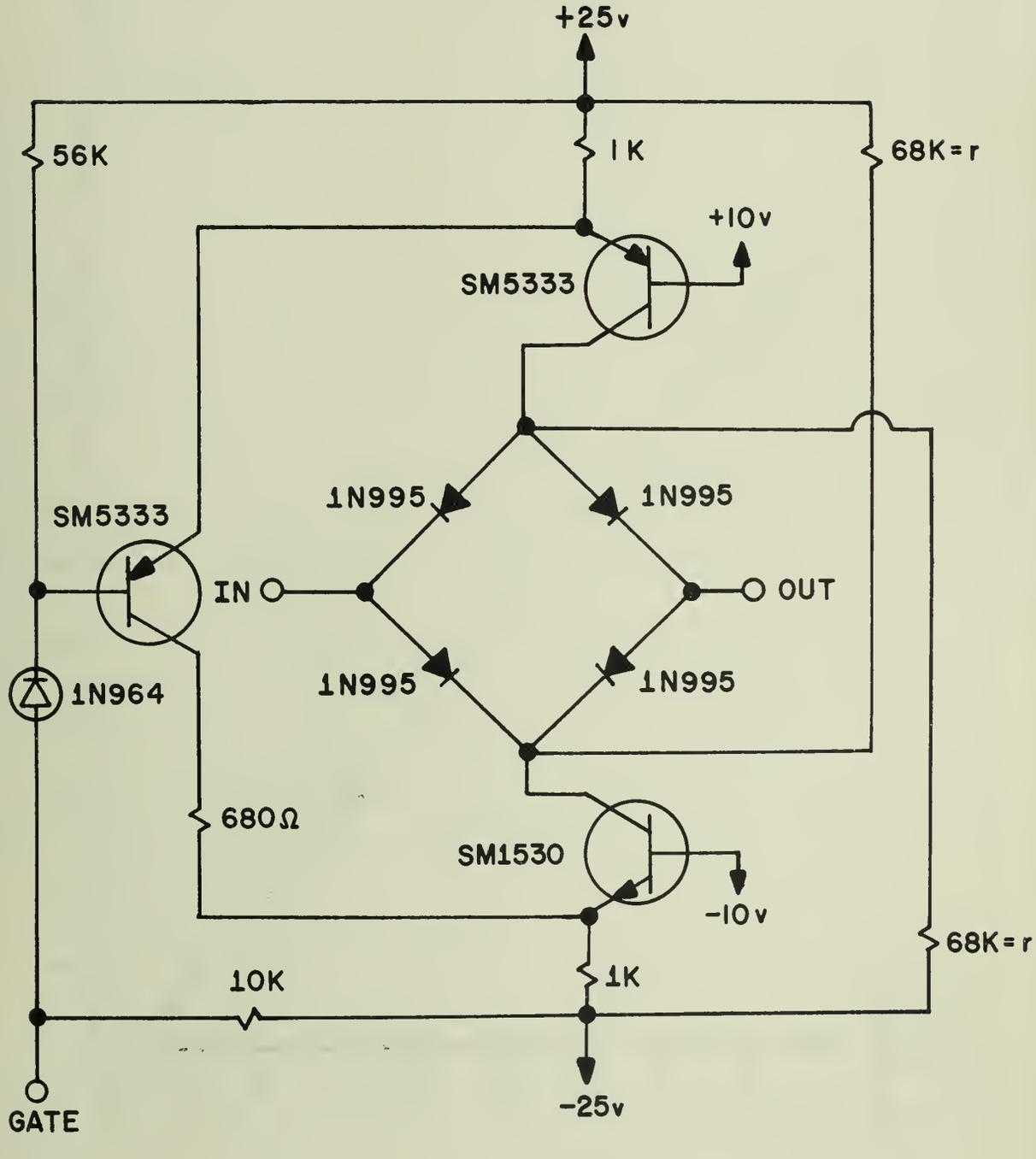


Figure 7. Diamond Gate for Paramatrix.

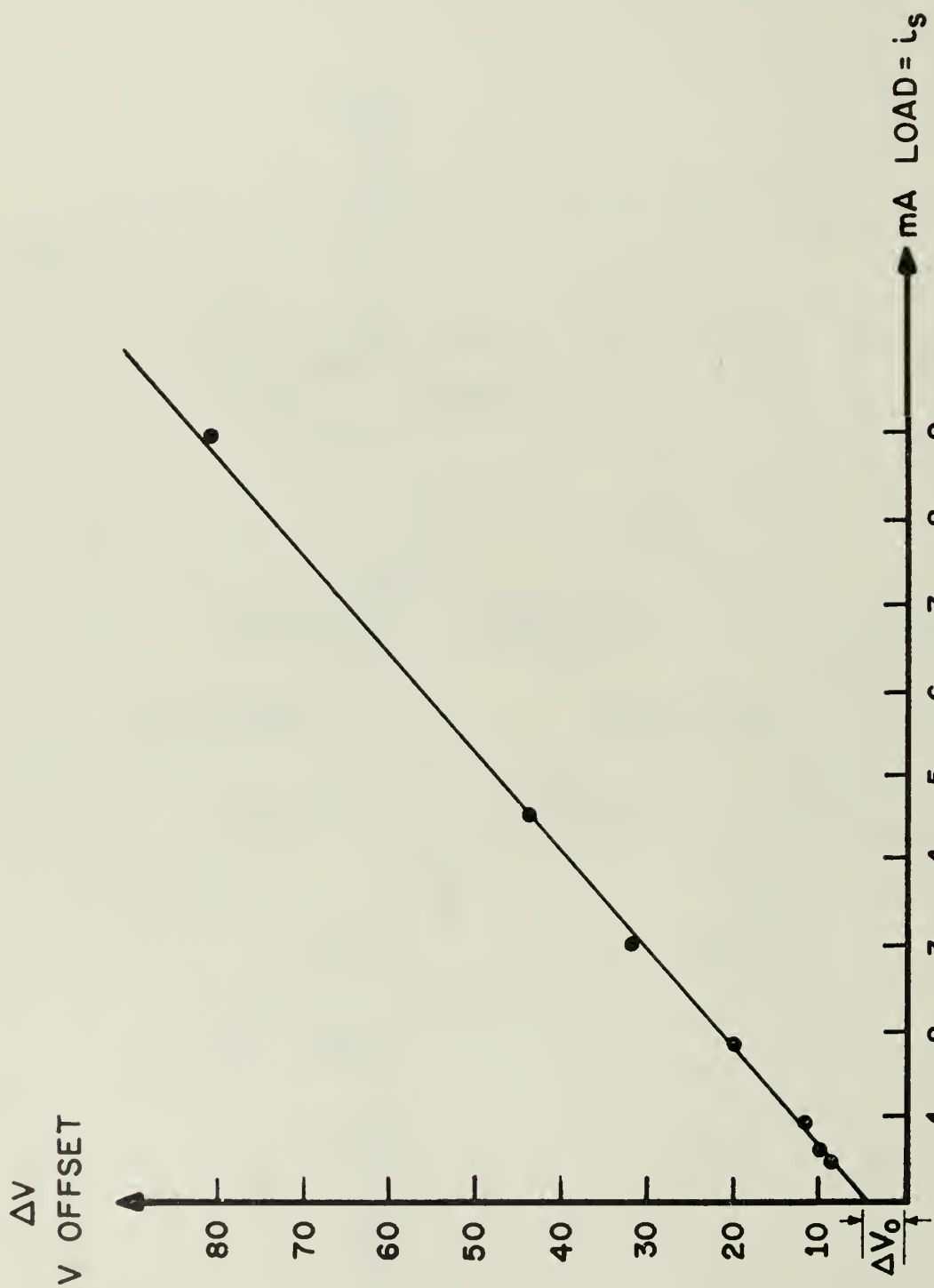


Figure 8. Graph of ΔV vs i_s.

is

$$R_{\diamond} = \frac{\Delta V - \Delta V_0}{\Delta i_s} = \frac{76}{9} = 8.2\ \Omega$$

i_s (ma)	0	1	2	3	4	5	6	7	8	9
ΔV (mv)	5	15	22	41	40	48	56	65	74	81

Table 1. Static Test Data for I_0 = 15 ma.

It is interesting to note that if we use Eq. (2.16) with r = 0, and $\frac{KT}{q} = \frac{1}{40}$, then the ideal figure of merit for I_0 = 15 ma is $R_{\diamond}$ = 6 Ω which, considering the approximations involved in the derivation, is a fairly good comparison.

The dynamic performance of the diamond is quite good. The rise time of the circuit is mainly a function of the bridge resistance and the junction capacitances of the bridge diodes and T_1 and T_2. Since the bridge resistance is very small the rise times are quite fast, typically on the order of 40 ns. The fall times however are a function of the junction capacitance and the output resistance of the bridge which is usually 1 to 2 K As a result the fall times are slower, typically 100 ns for a 1 K load. The addition of resistors, r, to the circuit have the effect of back-biasing the bridge when the bias current is removed and results in a faster fall time.

2.6 Diamond Gate with Gain

One last point should be brought out concerning the diamond gate as discussed in this chapter, namely, that it is a completely passive element. All of the current that is required by the load must be supplied at the input of the circuit.

Obviously it would be very desirable to have a gate which is capable of providing current gain. Some effort has been made to design such a circuit and the results have been favorable. The circuit of interest is shown in Figure 9.

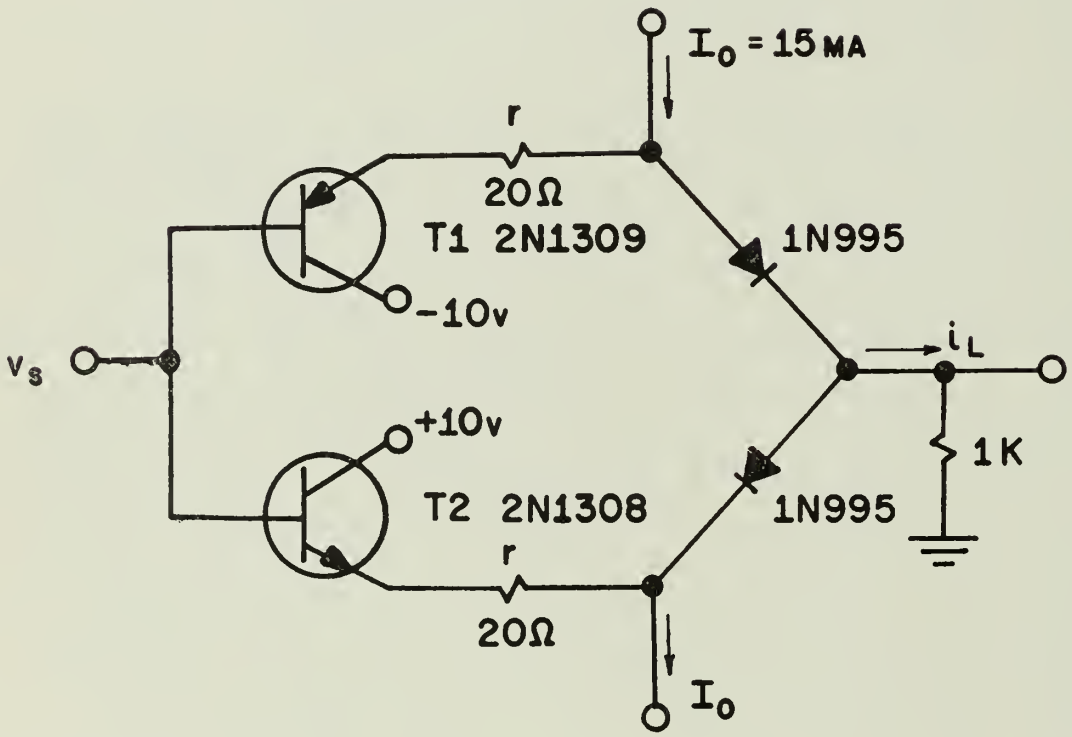


Figure 9. Transistorized Diamond.

The purpose of the small resistors, r, is to balance the right and left sides of the bridge in order that the bias current I_0 will split evenly when the input is at ground. This is necessary since the junction drop of the diodes is greater than the emitter-base drop of the transistors at 7.5 ma. The maximum offset observed in this transistor circuit is 180 mv at i_L = 8 ma. Though this offset seems high it is quite easily explained by considering the current change in resistor r. When v_s = 0 we have 7.5 ma

through T_1 and when $v_s = +8$ v ($i_L = 8$ ma) we have (from Eq. 2.9) approximately 3.5 ma through T_1 and since r is a linear element, the total voltage change across r alone is 80 mv.

Thus it can be seen that if r could be eliminated by obtaining transistors and diodes with matched junction drops at quiescent current, an offset of 100 mv or lower could be easily achieved. In this case the circuit of Figure 9 with its property of current gain would be very useful.

3. ANALOG COMPARATOR

The Paramatrix system required the design of an analog comparator circuit with two rather special characteristics. First, it was necessary to compare analog voltages over the unusually wide range of +8 to -8 volts and furthermore it was required that the sensitivity of the voltage comparison be adjustable over the range 0.2 to 2.0 volts. It was also desired that this sensitivity adjustment be voltage-controlled.

3.1 Differential Input Stage

The input stage for a comparator often consists of the differential connection shown in Figure 10. It has been shown in the literature[2] that if the input pair is driven by a constant-current source, the switching sensitivity is very high. In fact, if the emitter resistors, r, are set

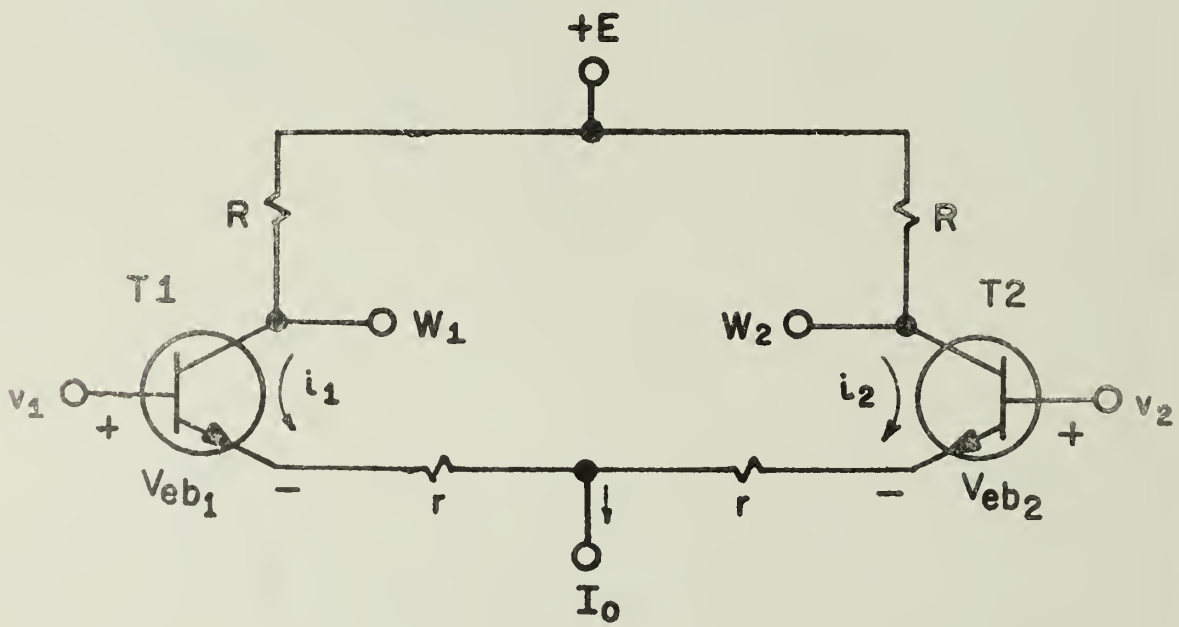


Figure 10. Comparator Input Stage.

equal to zero, then as small as a 0.1 v difference in inputs will switch about 90 per cent of the standing current I_0 through one transistor. If r is increased in both emitters equally, a larger voltage difference is required to achieve the same result. This phenomenon is shown graphically in Figure 11. It is sufficient to consider only the emitter-base junction characteristics since $|v_1 - v_2| = |v_{eb_1} - v_{eb_2}|$ for the case r = 0. For the case $r \neq 0$, one can obviously form a combined characteristic of the junctions in series with the resistance r (as shown).

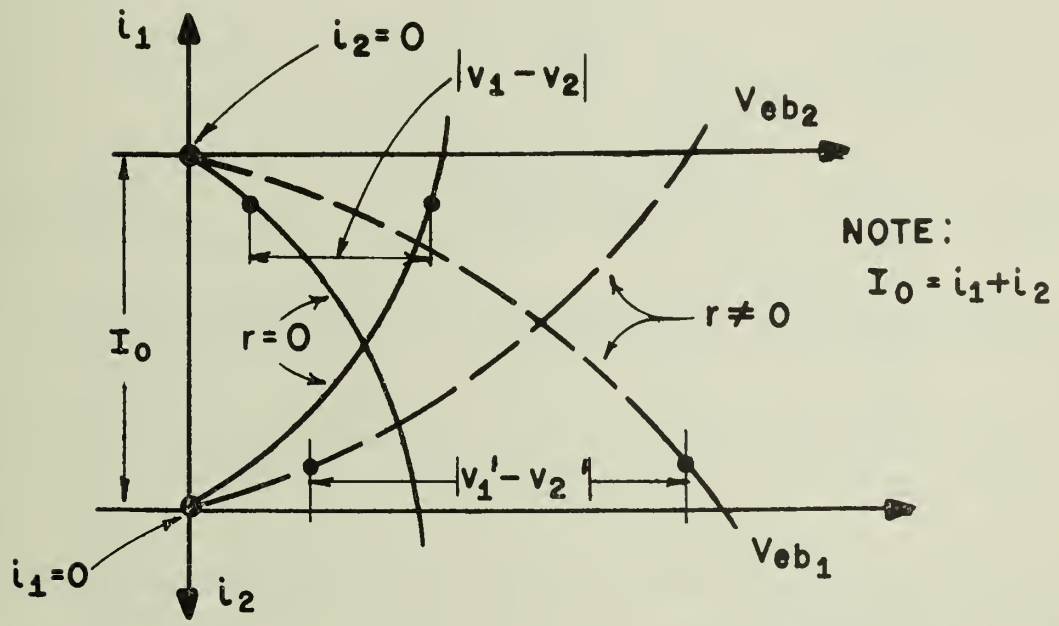


Figure 11. Graphical Analysis of Input Stage.

3.2 Linear Analysis of the Differential Stage

If we assume transistors T_1 and T_2 to be identical, d-c α's = 1, and neglect the emitter-base drops with respect to ir, then a linear analysis can be made of the differential stage. From consideration of Figure 10, it is clear that

$$0 \leq i_1,\ i_2 \leq I_0 \tag{3.1}$$

Hence letting $v_1 = v + \epsilon$ and $v_2 = v$, we have

$$v + \epsilon - i_1 r = v + i_1 r - I_o r$$

$$i_1 = \frac{I_0 r + \epsilon}{2r} \tag{3.2}$$

and from symmetry

$$i_2 = \frac{I_0 r - \epsilon}{2r} \tag{3.3}$$

Due to restrictions (3.1), the detectable input differences lie in the range,

$$-I_0 r \leq \epsilon \leq I_0 r \tag{3.4}$$

that is, the circuit saturates for all $|\epsilon| > I_0 r$. From Eqs. (3.2) and (3.3) the collector voltages become

$$w_1 = \epsilon \left(-\frac{R}{2r}\right) + E - \frac{RI_o}{2}$$

$$w_2 = \epsilon \left(\frac{R}{2r}\right) + E - \frac{RI_o}{2} \qquad (3.5)$$

It is instructive to consider Eqs. (3.5) and restriction (3.4) graphically, as shown in Figure 12. Due to the symmetry of these curves, it is

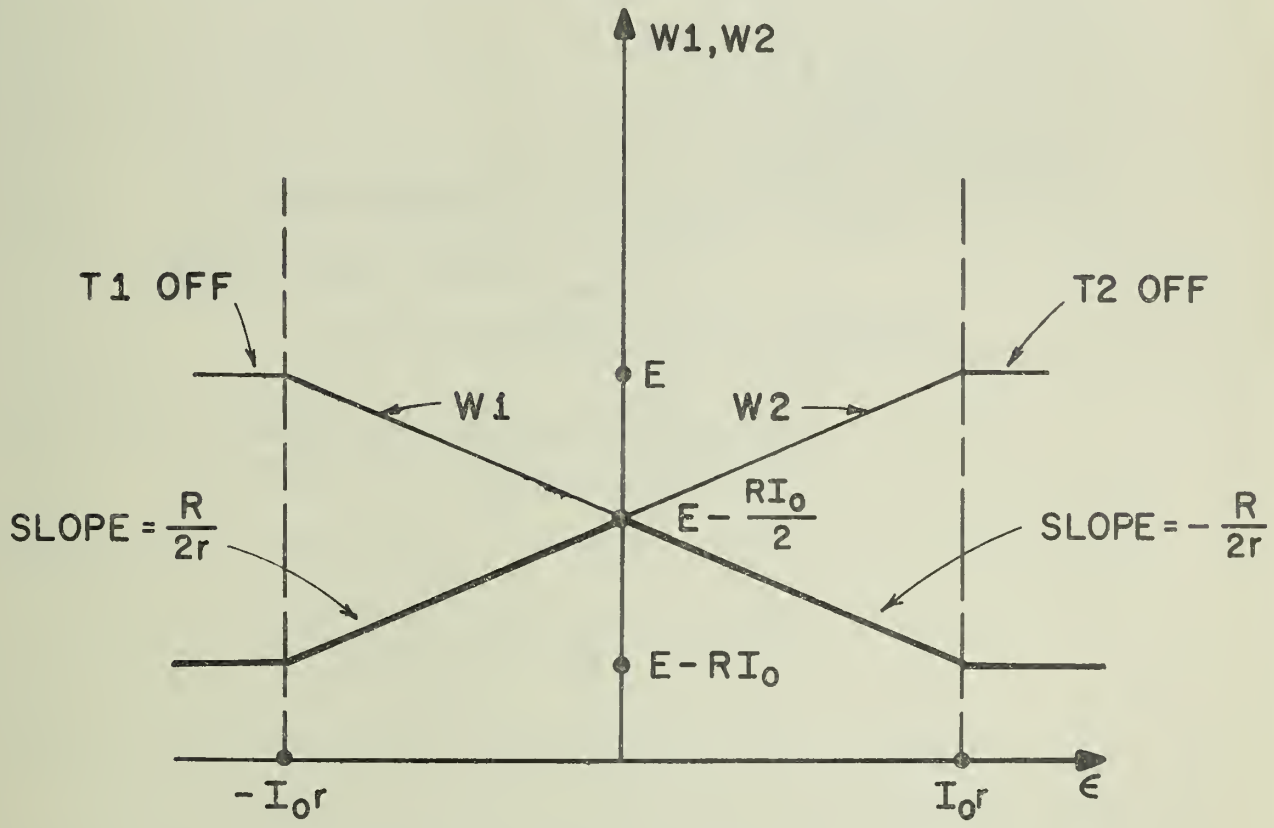


Figure 12. Graph of w_1, w_2 vs ϵ.

obviously not necessary to look at both collectors to determine coincidence or noncoincidence of the input signals. Clearly, it is sufficient to look at only the smaller of the collector voltages (i.e., min (w_1, w_2)) as shown by the darkened portion of the curves. Let us define

$$w = \min (w_1, w_2)$$

$$\eta = |\epsilon| \tag{3.6}$$

and

Hence the graph of Figure 12 can be simplified to that shown in Figure 13.

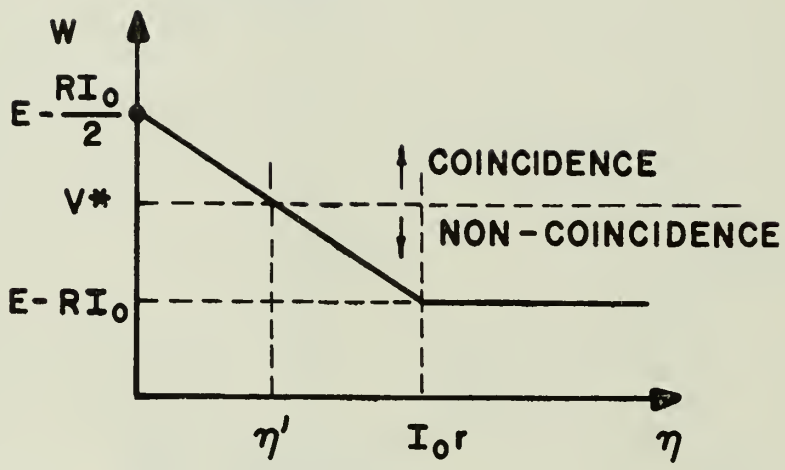


Figure 13. Simplified Graph.

It is useful at this point to assume a threshold voltage V* (which is in the range of w) and to define what we mean by coincidence and non-coincidence of input signals in terms of this voltage. The following are reasonable definitions

$$w \geq V^* \quad \text{means coincidence of input signals}$$

$$w < V^* \quad \text{means noncoincidence} \tag{3.7}$$

If $V^* = E - RI_0/2$ there is clearly only one point of coincidence, viz., $\eta = 0$. However, if $V^* < E - RI_0/2$, as illustrated in Figure 13, it is

possible to have coincidence for all $\eta < \eta'$. This latter point illustrates one method of achieving sensitivity control, i.e., adjustment of the threshold voltage.

3.3 Sensitivity Selection and Practical Design Considerations

In order to convert the differential amplifier to an analog comparator it has been pointed out that two modifications are necessary. First, a circuit is required which will respond only to the lowest of the collector voltages and second, some method is required to adjust the comparator sensitivity. While it has been shown that sensitivity selection can be achieved by varying the threshold voltage, V*, it is desirable from the standpoint of circuit efficiency to adjust sensitivity by varying w (Figure 13) with V* fixed throughout the sensitivity range.

A very elegant, yet simple circuit which will serve both of the above functions is the diode "or" circuit. The cathodes are connected to the collectors of the input transistors and the anodes are fed through a resistance to a variable supply, S. Varying S over the range

$$V^* \leq S \leq E \tag{3.8}$$

will result in the variation of η' over the range

$$0 \leq \eta' \leq I_0 r \tag{3.9}$$

In order to derive the final circuit equations we will analyze the circuit of Figure 14, again assuming ideal transistors and diodes. The analysis becomes somewhat simpler if we define the emitter currents as

$$i_1 = \frac{1}{2}(I_0 + i)$$

$$i_2 = \frac{1}{2}(I_0 - i)$$

and hence, $\epsilon = ri$.

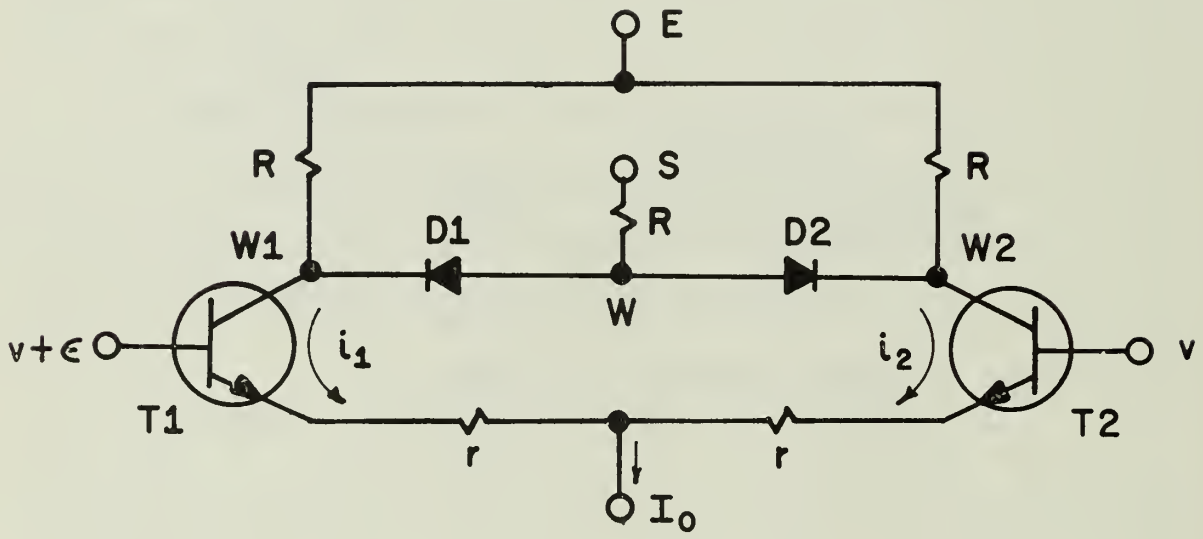


Figure 14. Modified Differential Amplifier.

Now with $\epsilon > 0$ we assumed D_1 on and D_2 off, so that

$$w = w_1 < w_2$$

Then, writing KCL equations at w_1, we have

$$\frac{1}{2}(I_0 + i) = \frac{1}{2}(I_0 + \epsilon/r) = \frac{E - w_1}{R} + \frac{S - w_1}{R}$$

or

$$w_1 = w = \frac{1}{2}(E + S) - \frac{1}{4}R(I_0 + \epsilon/r) \tag{3.10}$$

Thus if it were true that only one diode were on, w as a function of $\eta = |\epsilon|$ and S would appear as shown in Figure 15. (This should be compared to Figure 13.) The sensitivity selection property of the modified circuit is obvious. Of course it is not always true that only one diode is on at a time; with $\eta = 0$ both diodes are on. Then $w = w_0$, say, which is given by

$$I_0 = \frac{2E + S - 3w_0}{R}$$

or

$$w_0 = \frac{1}{3}(2E + S - RI_0) \tag{3.11}$$

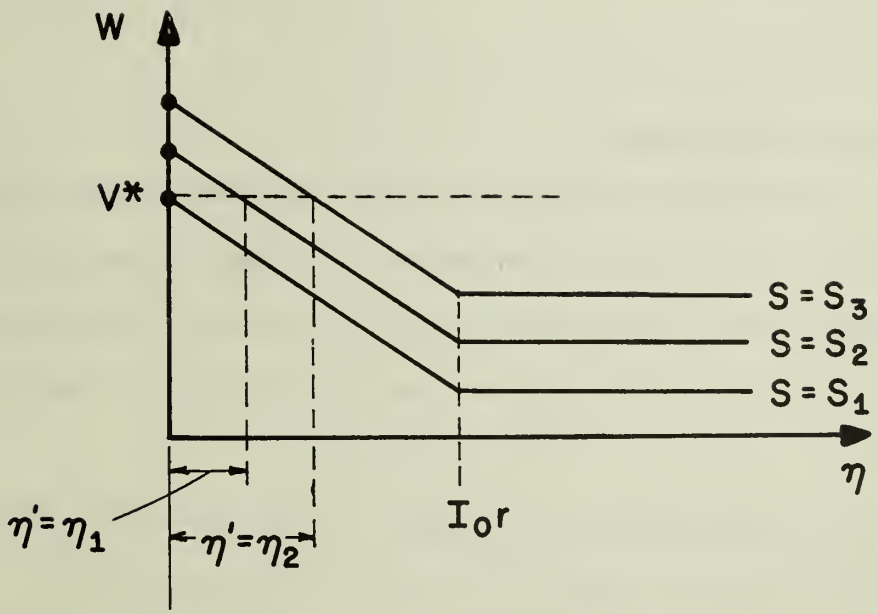


Figure 15. Modified Differential Amplifier Response.

Depending on the magnitude of S, w_0 can be either greater or less than the limit of w as $\epsilon \to 0$ in Eq. (3.10). Furthermore, let us calculate w_2 on the assumption that D_2 is off:

$$\frac{1}{2}(I_0 - i) = \frac{1}{2}(I_0 - \epsilon/r) = \frac{E - w_2}{R}$$

or

$$w_2 = E - \frac{1}{2} R(I_0 - \epsilon/r)$$

Then

$$w_2 - w_1 = \frac{1}{2}(E - S) - \frac{1}{4} R(I_0 - \frac{3\epsilon}{r}) \qquad (3.12)$$

which shows that, if $\epsilon < \frac{1}{3} r I_0$ and (E - S) is small enough, it is not necessarily true that $w_2 > w_1$. In this case we have $w_1 = w_2 = w_0$, even though $\eta \neq 0$.

3.4 Specific Requirements

As previously discussed, we must now choose some threshold voltage V* from the range of possible values of w and make the definitions as given in Eq. (3.7). Then varying S alters the value of η' (recall that for all $\eta < \eta'$ the inputs are the same) and hence provides our sensitivity selection.

It is convenient to set $S_{max} = E$ and $S_{min} = V^*$. We also require that, for S = E and $\epsilon = rI_0$, w = V*. Hence from Eq. (3.10)

$$V^* = \frac{1}{2}(E + E) - \frac{1}{4} R(I_0 + I_0)$$

or

$$RI_0 = 2(E - V^*) \tag{3.13}$$

We notice that, for $S = V^*$ and RI_0 given by (3.13), Eq. (3.11) gives

$$w_0 = \frac{1}{3}(2E + w - 2E + 2w) = w$$

which is due to choosing the sensitivity resistor equal to the collector resistors.

Finally substitution of Eq. (3.13) in Eq. (3.12) gives

$$w_2 - w_1 = \left(\frac{3R}{4r}\right) \epsilon - \frac{1}{2}(S - V^*)$$

Hence the on-off diode condition is satisfied if

$$\eta > \frac{2r}{3R}(S - V^*) \tag{3.14}$$

3.5 Analog Comparator for Paramatrix

The comparator circuit which was designed for the Paramatrix system is shown in Figure 16. For this circuit the emitter of T_3 is tied to the threshold voltage $V^* = 10$ v and the digital output signal is taken off the collector of T_4. Hence for coincidence $w > 10$ v and $v_o = 0$ v; for noncoincidence $w < 10$ v and $v_o = -5$ v. We also have from Eq. (3.11)

$$w_0 = \frac{1}{3}(20 + S)$$

if both diodes are on. From Eq. (3.10) for only one diode on we have

$$w = 5 + \frac{1}{2}S - 3.75\eta \tag{3.15}$$

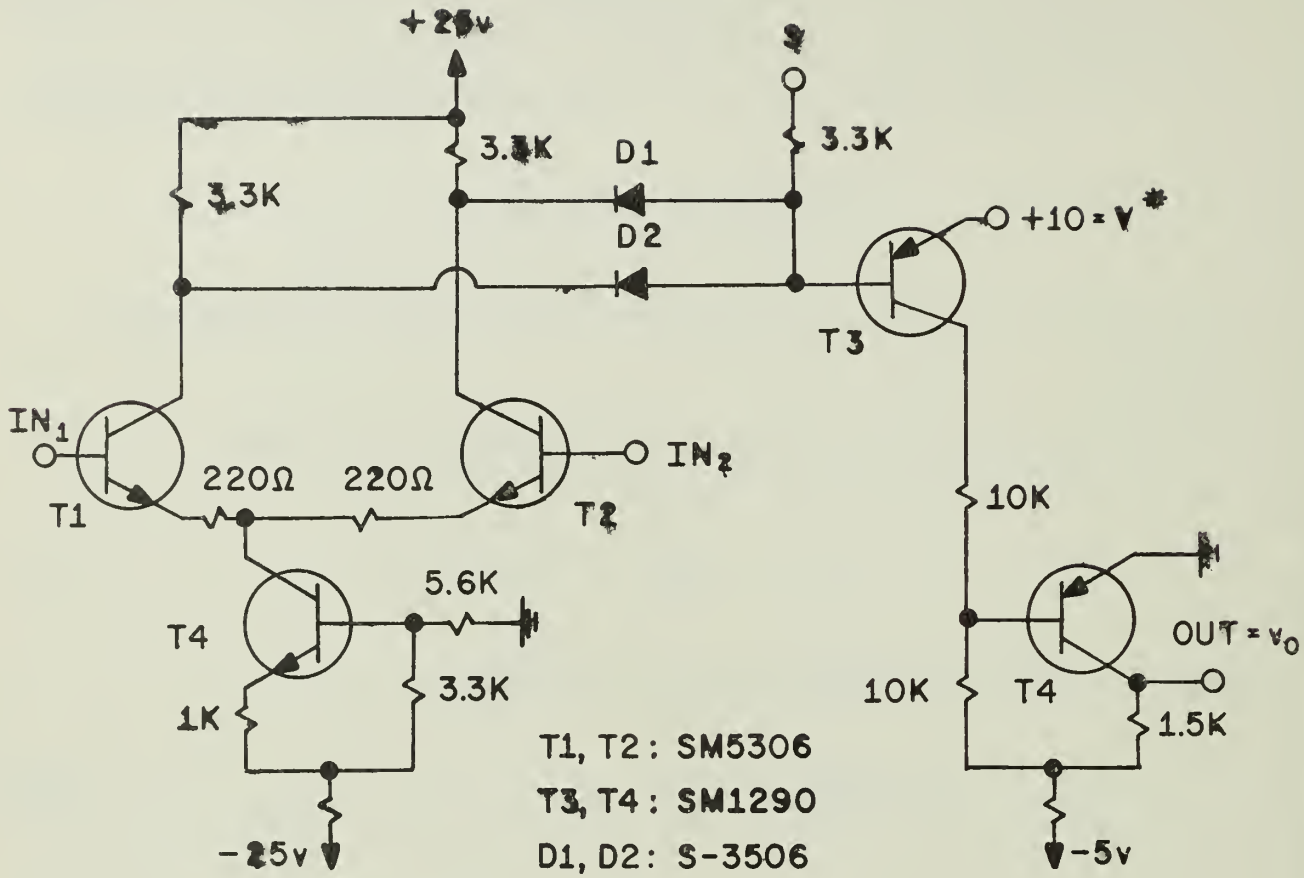


Figure 16. Paramatrix Comparator.

and finally for (3.15) to be true we require that

$$\eta > \frac{2}{45}(S - 10) \tag{3.16}$$

These results are illustrated graphically in Figure 17. It will be noticed that the case of both diodes conducting ($w = w_0$) for noncoincident input signals occurs only at S = 10 v, i.e., $\eta' = 0$.

Naturally the foregoing analysis of the comparator circuit has been an ideal one. In the real world the curves of Figure 17 would be different since transistors do not have infinite β's, junction drops are not

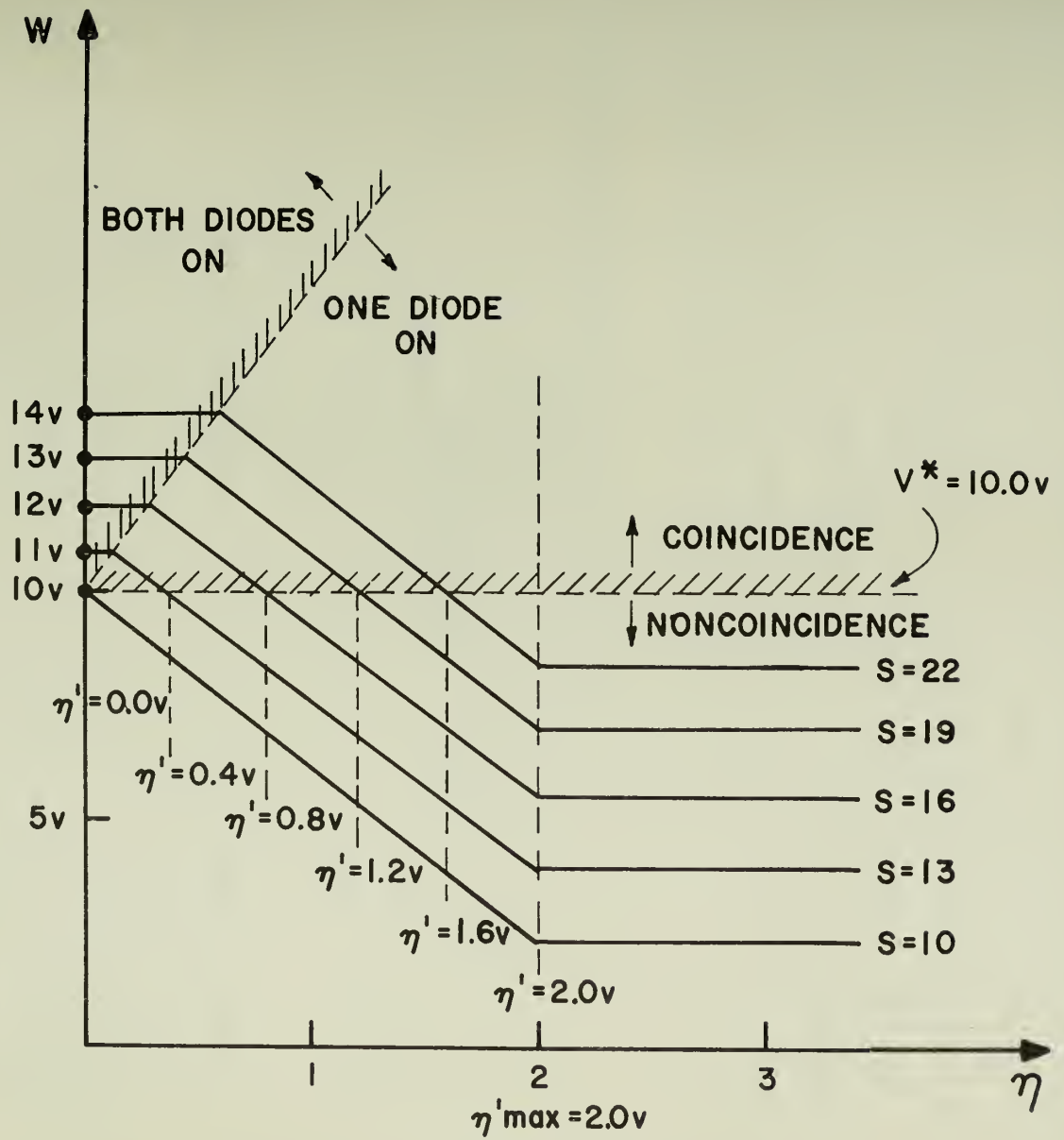


Figure 17. Ideal Comparator Characteristics.

zero and thresholds cannot be defined exactly. However these effects can be somewhat reduced when necessary by using higher currents and voltages.

The circuit of Figure 16 approaches quite closely the characteristics of Figure 17 except at the extremes of the sensitivity voltage S where we would expect the real curves to be quite rounded. The experimental sensitivity data for the Paramatrix comparator is given in Table 2.

S	η'
10 v	No coincidence
12 v	0.2 v
13 v	0.38 v
16 v	0.78 v
19 v	1.25 v
22 v	1.65 v
24 v	2.0 v
25 v	No noncoincidence

Table 2. Experimental Data for Paramatrix Comparator.

4. APPLICATIONS OF HYBRID CIRCUITS

4.1 Circuit Requirements and Notation

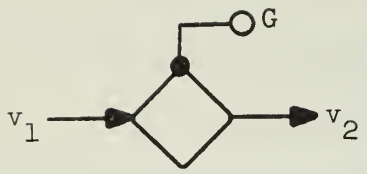
The applications suggested by W. J. Poppelbaum, which we are about to discuss, will require the use of the analog comparator, the diamond gate, and a low-offset current amplifier which we will call a compensated emitter-follower. This latter device has been designed for the Paramatrix system and is described in Appendix A. When a compensated emitter-follower is used at the input of a diamond gate the resulting device is a diamond gate with current gain (essentially equivalent to the circuit of Figure 9). Clearly, in this case, the requirement that the diamond be driven from a low-impedance source is substantially relaxed.

The basic block diagrams which will be used in the following discussions are shown in Figure 18.

4.2 Paramatrix Digital-to-Analog Conversion

The term digital-to-analog conversion normally means that one digital pulse is considered equivalent to a preset d-c voltage V_0. A chain of n digital pulses at the input of a digital-to-analog converter will result in a d-c output of nV_0, independent of the time at which the pulses occur.

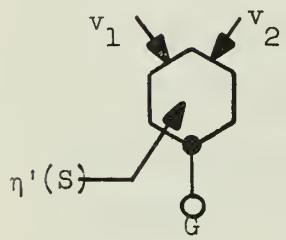
In the Paramatrix system the term digital-to-analog conversion carries a slightly different connotation, namely that one digital pulse depending on where it occurs in time (relative to the system clock) will produce one predetermined analog level during the duration of the pulse. Possibly a more descriptive name for this would be digital-to-sampled-analog conversion. The basic layout of the Paramatrix digital-to-analog converter is shown in Figure 19 together with the output waveshapes which



when G = 1, $v_2 \simeq v_1$

when G = 0, v_2 floats

(a) Diamond Gate

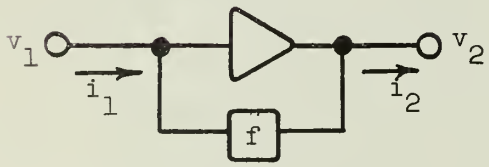


when $|v_1 - v_2| \leq \eta'$, G = 1

when $|v_1 - v_2| > \eta'$, G = 0

$\eta'(S)$ = comparator sensitivity as a function of sensitivity voltage (as in Figure 16)

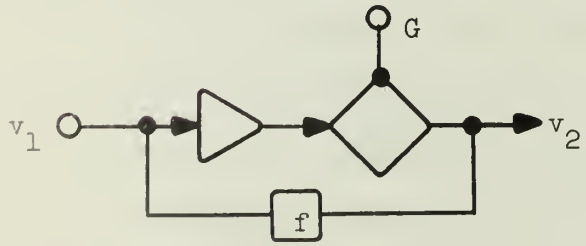
(b) Analog Comparator



$v_2 = v_1$

$i_2 \simeq \beta i_1$

(c) Compensated Emitter-Follower

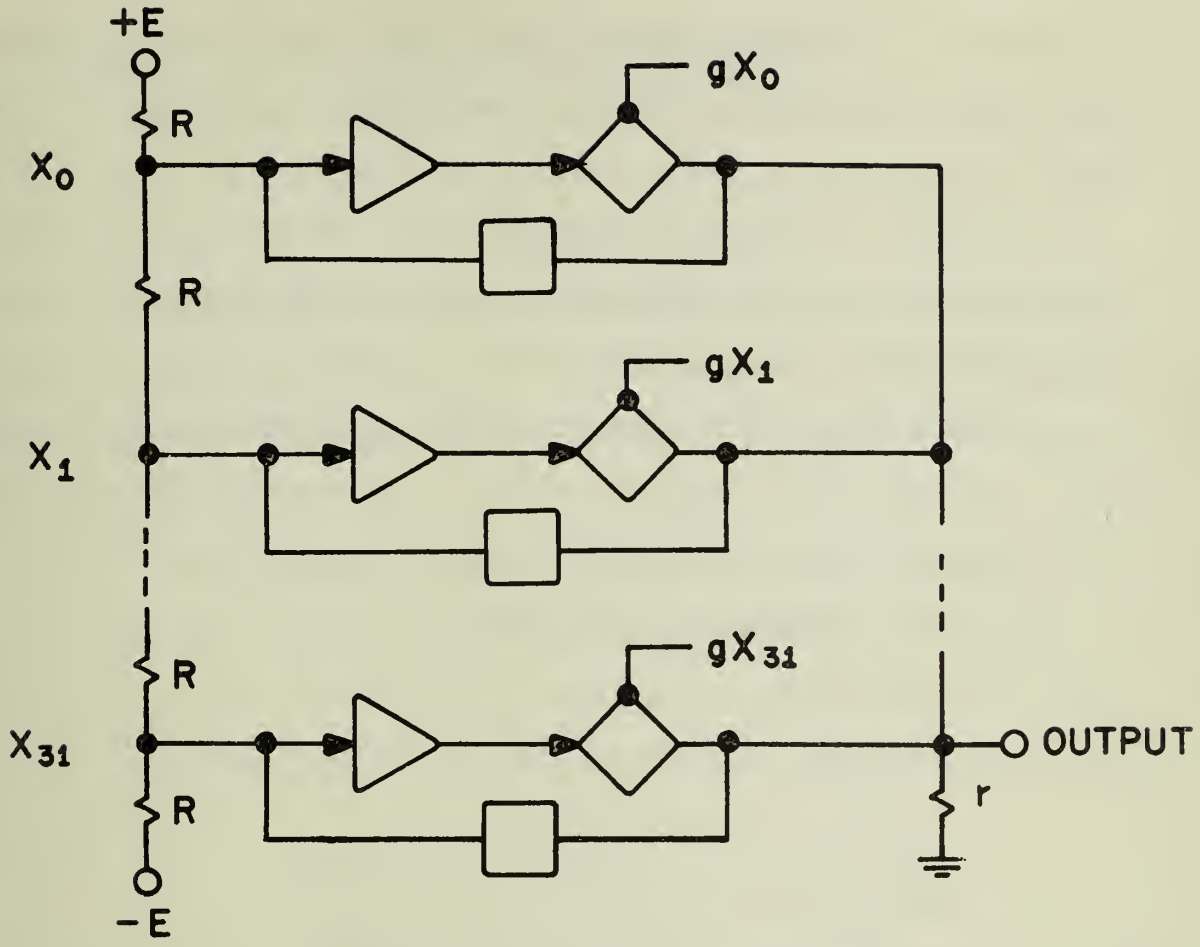


when G = 1, $v_2 \simeq v_1$

when G = 0, v_2 floats

(d) Diamond Gate with Current Gain

Figure 18. Circuit Notations.



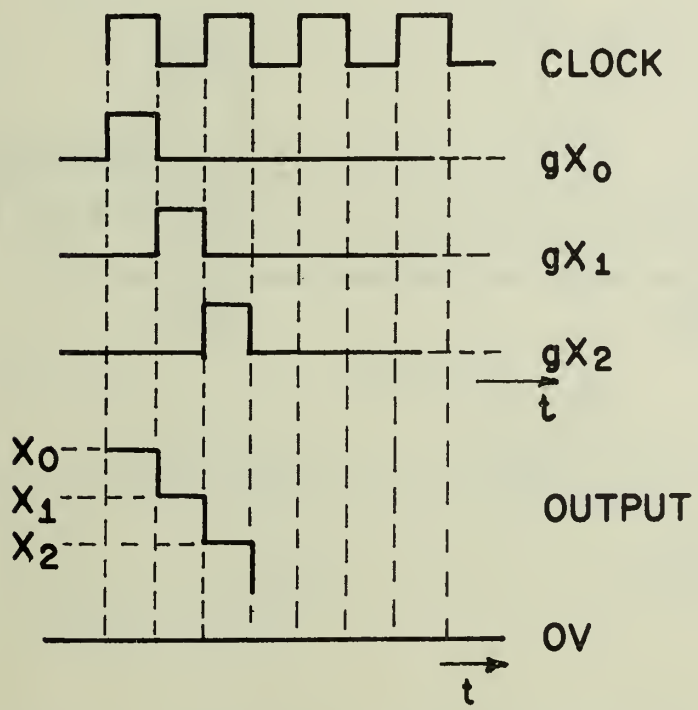


Figure 19. Paramatrix D/A Converter and Waveshapes.

are produced. The gating signals gX_i are decoded clock times and since they do not overlap, only one analog voltage exists on the output bus at a time.

As was described in the introduction to this thesis, the output of the Paramatrix system is displayed on a 32 x 32 matrix which is scanned by the system clock. Thus to each coordinate corresponds two digital signals gX_i, gY_j and, by means of the digital-to-analog converter of Figure 19, each matrix coordinate also corresponds to a set of analog levels X_i, Y_j. These analog voltages are the signals which serve as the inputs to the transformation circuitry. An illustration of this is given in Figure 20.

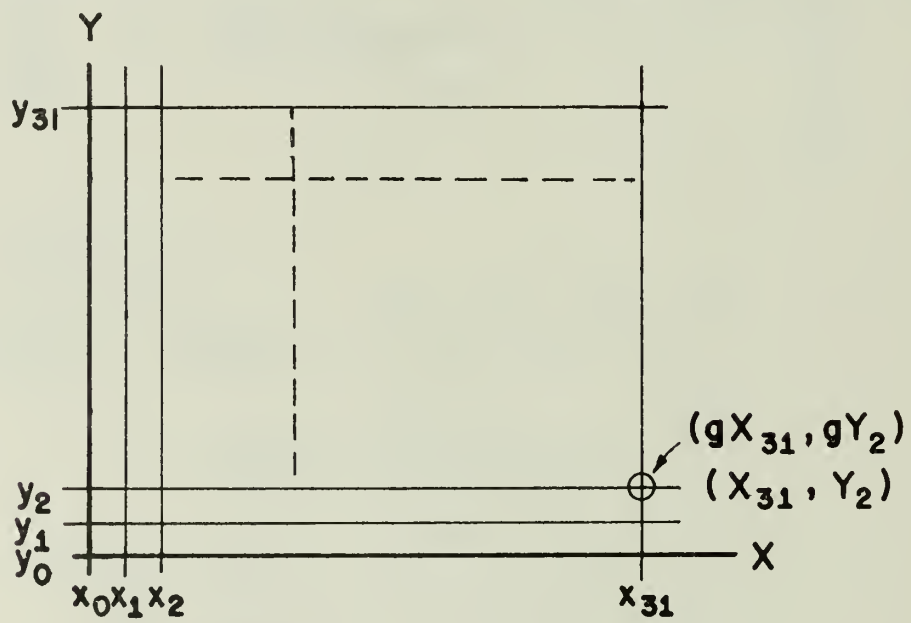


Figure 20. Matrix-Coordinate Representations.

4.3 Paramatrix Function Generation and Interpolation

The input information to Paramatrix consists of voltage levels in the range -8 to +8 volts which have been set on potentiometers, one potentiometer for each of the 32 columns of the matrix. Hence at each column x_i we have potentiometer voltage setting $F(x_i)$. As discussed in Section 4.2, to any coordinate x_i there corresponds a reference voltage X_i and hence the equivalence of 32 x columns to 32 quantized reference voltages is apparent.

A simple look-up system by which one can find $F(x_i)$ provided its x coordinate is known through its voltage analog X_i, is shown in Figure 21. In this device if X* is an exact x coordinate (say $X^* = X_i$), it will compare with only one quantized reference level, namely X_i, provided

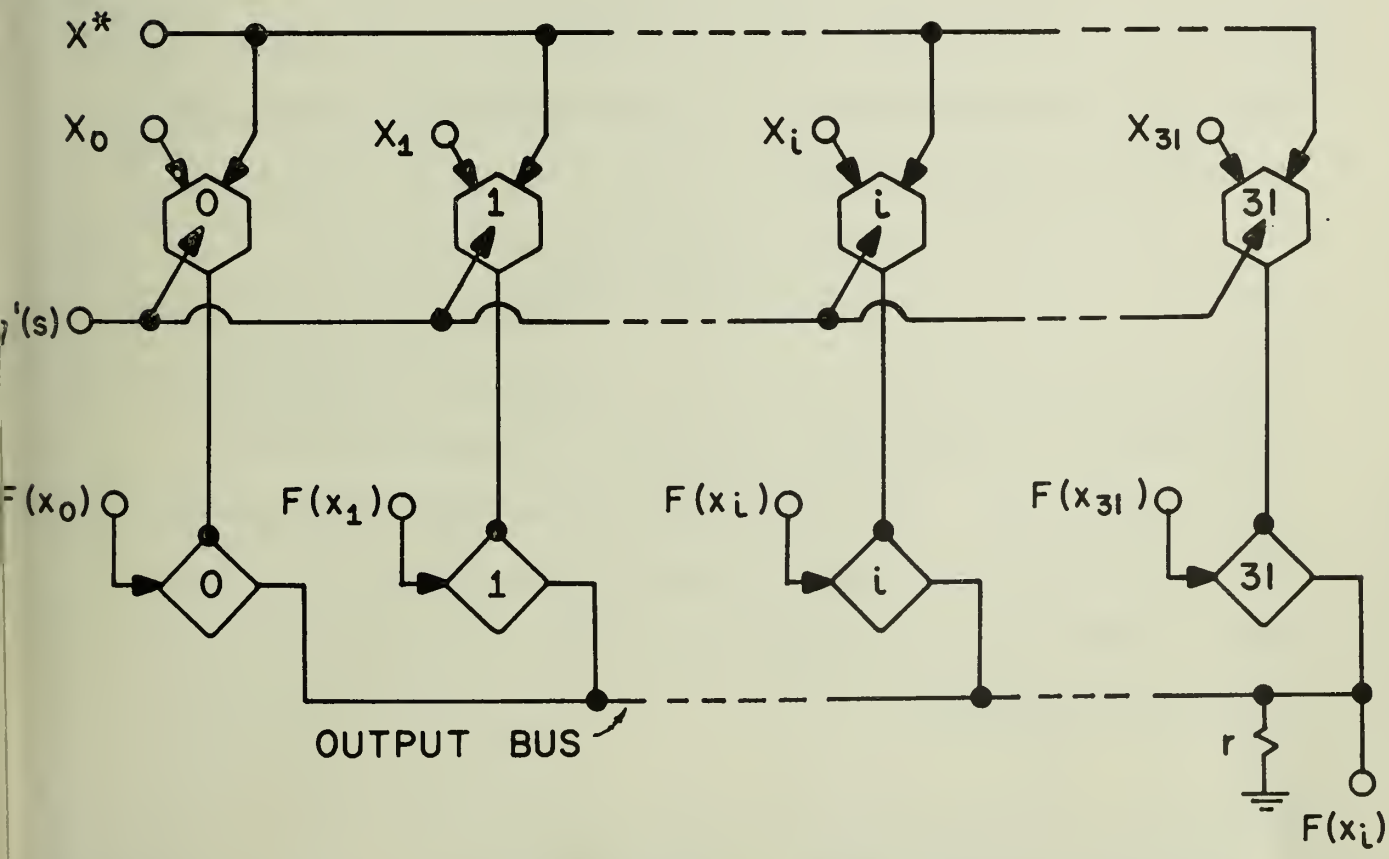


Figure 21. Look-up System.

$$\eta'(S) < \frac{1}{2} |X_i - X_{i-1}|$$

When the comparison is made, comparator i will give a "1" output signal which will gate the potentiometer set to $F(x_i)$ onto the output bus. The potentiometer settings in the above essentially constitute the input program.

The above discussion applies only in the case when the Paramatrix system is being used as a pattern copying device, i.e., the output reference frame is identical to the input frame and no transformation is performed. In the case where the input picture undergoes a transformation, it is no longer true that the common input to all of the comparators will be in exact correspondence to one of the reference levels.* In this case, calling the common input X*, it is true that

$$X_j \leq X^* \leq X_{j+1} \tag{4.1}$$

since all of the analog voltages lie in the same bounded interval. Due to Eq. (4.1) we can postulate that

$$F(x_j) \leq F(x^*) \leq F(x_{j+1}) \tag{4.2}$$

Equation (4.2) may certainly not be true; however, it is one possible approximation for a functional value which is not available on our input potentiometers. This approximation assumes that the total function composed of the 32 $F(x_i)$'s has no discontinuities in the regions between any two reference levels. This is of course a reasonable assumption.

---

* The reason for this will not be explained here; however, the subsequent discussion should be clear without it.

One method of selecting a value for $F(x^*)$ is to assume that

$$F(x^*) = \frac{F(x_j) + F(x_{j+1})}{2} \tag{4.3}$$

Obviously Eq. (4.3) is just a simple linear interpolation between $F(x_j)$ and $F(x_{j+1})$, one approximation of the many that could be made.

The advantage of this approximation lies in its ease of implementation. The system of Figure 21 is easily modified by the addition of the voltage averaging network as discussed in Appendix B. The output of this network for the case n = 2 is

$$V = \frac{V_1 + V_2}{2} \qquad \text{for } r \gg R$$

It is clear that since the output of the ungated diamond will float (assume the voltage of the common bus) the resistor network will appear as two small resistors terminated in a very large resistance. It is also evident that exact comparisons can still be made with this modification. This modified look-up and interpolation system is shown in Figure 22.

In order to achieve the desired output of Eq. (4.3) the setting of $\eta'(S)$ must be such that X* will compare to only two reference levels. Hence

$$\eta'(S) < |X_i - X_{i-1}|$$

will be satisfactory.

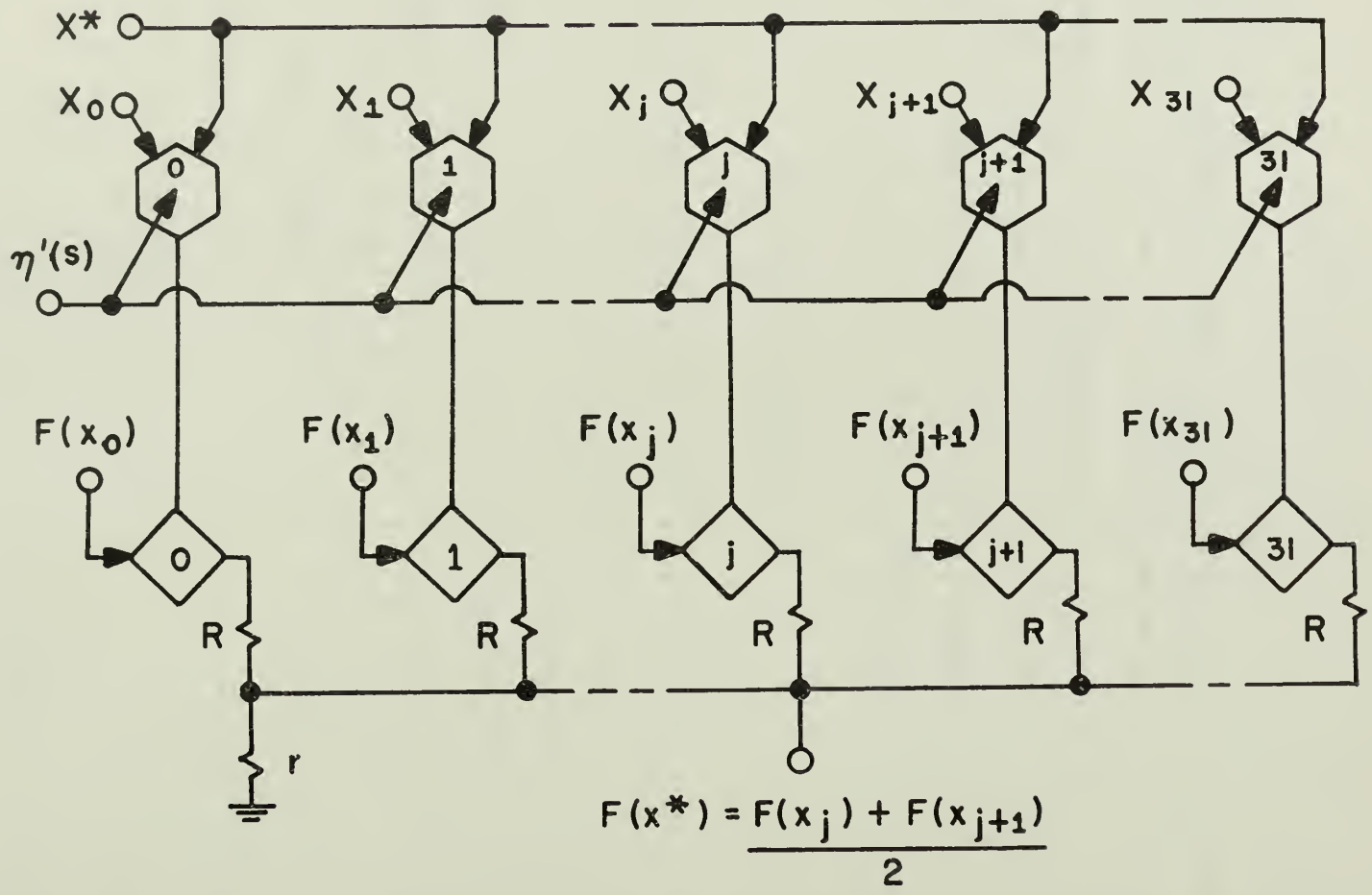


Figure 22. Look-up System Modified for Interpolation.

5. SUMMARY AND CONCLUSIONS

In this thesis we have attempted to present in some detail the design of two useful analog-digital circuits. The particular design criteria were derived from the requirements of the special-purpose pattern-processing computer called Paramatrix. It is felt that the circuit theory that has been developed is sufficient to enable the reader to design modified versions of these circuits to fit his own needs.

It is quite possible that the reader's circuit requirements are not as stringent as those of the Paramatrix system. In this case the circuit design could become substantially simplified. For example, if the signal levels to be gated by the diamond are small and/or a larger offset than say 100 mv can be tolerated then clearly the constant-current bias would not be necessary.

The reason for the use of Bypass-Gating for switching the diamond is to avoid the necessity of using a large supply to turn off the current-driving transistors. But Bypass-Gating is an inefficient method of switching as it requires that the large bias-current flow continuously. A more efficient method of gating can be achieved by the phasing-splitting amplifier as shown in Figure 23 (with suitable circuitry for driving the base of T from logic signal levels). With this method power will be absorbed by the diamond gate only during gating time.

The analog comparator is a special purpose circuit. Most comparator requirements are for threshold-type circuits where each comparator circuit is set to "flip" at some preset level which is made one of the inputs. Clearly the comparator circuit which is discussed here will perform this function with a few simple modifications.

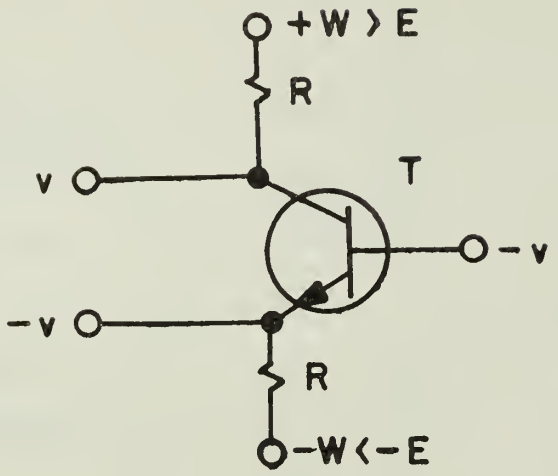


Figure 23. Phase-Splitting Amplifier.

The circuit applications which have been discussed are just two of many applications of hybrid circuitry; they have been presented chiefly for the purpose of tying-in the design discussions. Again these applications are special purpose.

A word must be said concerning the method of analysis used in deriving the circuit design equations. The seeming lack of the use of equivalent circuits in our analysis (although we have used a very ideal equivalent circuit) is easily justified. Our main interest is to design practical circuits to meet specific requirements. Design equations for such circuits can be derived by using less than ideal equivalent circuits for our models; however, to get simple equations which can be realized, one usually resorts to idealizing transistor parameters. We have used this simplifying procedure as the starting point of our analysis.

Finally it is certainly worth noting that many interesting extensions of these circuits could be pursued. For example one version of a transistorized diamond has been discussed; if the expense can be tolerated, the use of complimentary transistors (within a single case) to form the input would make this a very versatile circuit.

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APPENDIX A

Compensated Emitter-Follower

A compensated emitter-follower is essentially an amplifier with unity voltage gain and current gain relatively equal to β. There are a number of different methods of designing such a circuit one of which is to build a very high gain voltage amplifier and to reduce the gain to unity by means of voltage feedback. Another method is to use conventional emitter-followers in complementary connections and by means of current feedback reduce the voltage offset of the circuit to zero. The former design philosophy was used by M. Faiman in designing a compensated circuit for Paramatrix. The resulting topology is shown in Figure 24.

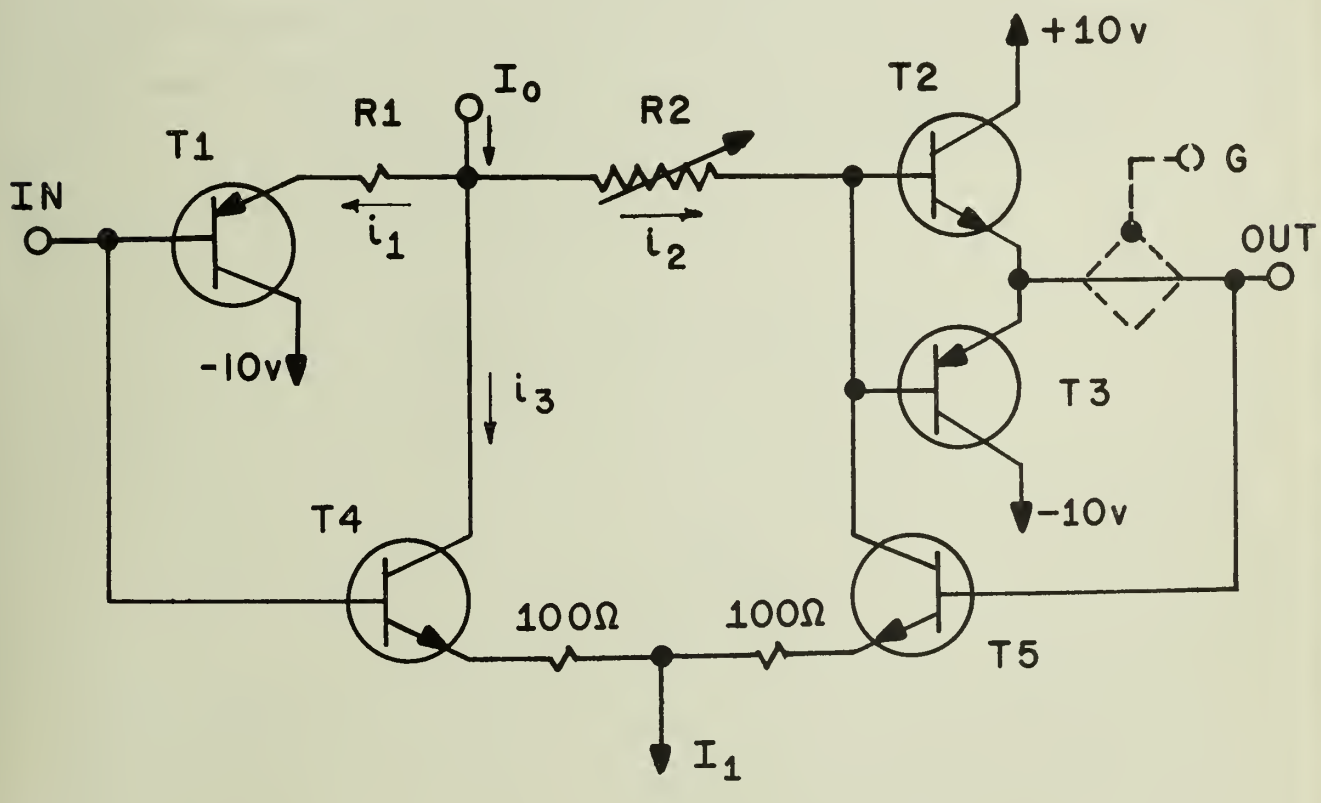

Figure 24. Compensated Emitter-Follower.

Clearly from Figure 24 (again assuming ideal transistors) since I_0 and I_1 are constant current sources, we have

$$I_0 = i_1 + i_2 + i_3$$

and

$$I_1 = i_3 + i_2 .$$

Hence,

$$i_1 = \text{constant} \qquad \text{(A.1)}$$

and the only circuit variation that must be compensated for is the variation of V_{eb} in the output transistors. This compensation is achieved by the varying of the current i_2 through R_2 by means of the differential amplifier composed of T_4 and T_5 in the feedback loop.

APPENDIX B

Derivation of Resistor Network for Voltage Averaging

For the purpose of the derivation we assume the topology of Figure 25.

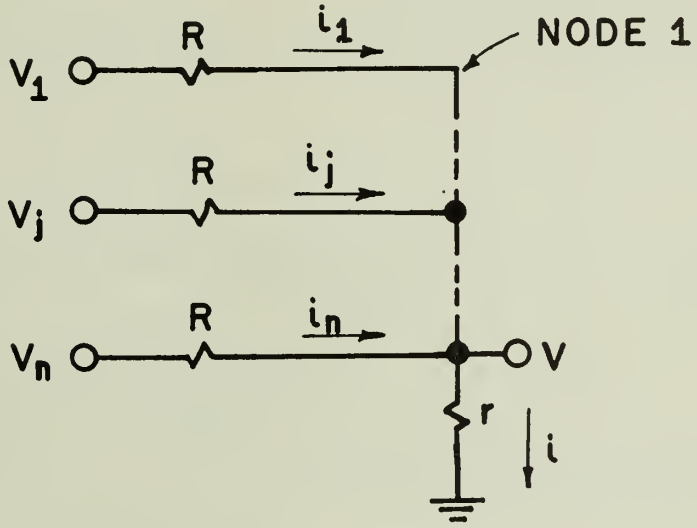

Figure 25. Topology for Voltage-Averaging Network.

Writing KCL at node (1), we have

$$\frac{1}{R}\sum_n (V_j - V) = \frac{V}{r} = \frac{1}{R}\sum_n V_j - \frac{n}{R} V$$

Hence,

$$V = \frac{\sum_n V_j}{(n + \frac{R}{r})} \qquad \text{(B.1)}$$

If we require in Eq. (B.1) that $r \gg R$

$$V \simeq \frac{1}{n}\sum_n V_j$$

Therefore the output voltage becomes the average of the input voltages.

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13. ABSTRACT

In order to design an analog/digital computer to perform pattern processing, it became necessary to design precision analog and analog/digital circuits. This paper discusses in detail the design of two hybrid circuits, namely an analog comparator and an analog gate. The design of a compensated emitter-follower is also described as are the applications of these three circuits in the Paramatrix, pattern-processing computer.

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